

		Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

U.S. GOVERNMENT PATENT APPLICATION		O.I.P.E.	PATENT DATE
AK Anz		Q.A. 11	
SCANNED			

APPLICATION NO. 09/684868	CONT/PRIOR	CLASS 365 716	SUBCLASS 17	ART UNIT 2818 112	EXAMINER D.L.
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Daniel Watkins

Diagnostic architecture using FPGA core in system on a chip design

TITLE

PTO-2040
12/89

ISSUING CLASSIFICATION

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	(Assistant Examiner) _____ (Date)				
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____				ISSUE FEE	
	(Primary Examiner) _____ (Date)			Amount Due	Date Paid
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